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# Final Report

for the entire contract period from February 1, 1992 to January 31, 1994

## Microstructure and Epitaxy in Oxide Superconductor Thin Films and Devices

Air Force Office of Scientific Research

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## Introduction

This report summarizes the work performed at the Pennsylvania State University (PSU) and the Westinghouse Science and Technology Center (WSTC) under the project entitled "Microstructure and Epitaxy in Oxide Superconductor Thin Films and Devices", AFOSR Grant # F49620-92-J-0159, under the direction of the principal investigator, Prof. A. H. Carim. The total period of the project was from February 1, 1992 to January 31, 1994. Results over the first year of the award, from February 1, 1992 through January 31, 1993, were summarized in the annual (interim) report submitted earlier. The present document will therefore focus on the more recent activities during the second year of the project.

The original graduate student assigned to this project, Gretchen L. Skofronick, received her M.S. degree in Ceramic Science and left the university in spring 1993. She is now employed by Los Alamos National Laboratories. Shortly thereafter, another student - Marjorie McGaughey - was selected to participate in this work. Ms. McGaughey also completed her M.S. (in Metals Science and Engineering) in the spring of 1993 and continued at Penn State through January 1994 under the direction of the P.I. The work described below was that which was undertaken by Ms. McGaughey, who also contributed substantially to the preparation of this report.

The objective of this work was to characterize microstructural aspects of device structures based on oxide superconductor thin films. The deposition and patterning of the films was carried out at WSTC under the direction of Dr. John Talvacchio. Preparation and, in some cases, initial examination of samples for transmission electron microscopy was performed at PSU. Because of the instrumental limitations at PSU, the bulk of the microscopy was performed at WSTC, where a versatile high-resolution instrument (Philips CM30) is available for such studies.

The specific devices chosen for microstructural evaluation during the past year were step-edge and edge S-N-S junctions incorporating  $\text{YBa}_2\text{Cu}_3\text{O}_{7-x}$  (YBCO) as the superconducting component and gold (Au) as the normal conductor. In development of these devices at WSTC, it was observed that the quality from one junction to the next was inconsistent. The YBCO tended to form continuously across the junction, causing a short-circuit, instead of being discontinuous as expected and desired. An undercut method was introduced to try to eliminate this problem and produce junctions with discontinuous YBCO.

Preliminary evaluation of chips processed with an undercut demonstrated that their behavior was still inconsistent and unsuitable for use. Electrical testing showed that each edge junction carried different amounts of current. It was decided that further structural analysis with the transmission electron microscope (TEM) was necessary in order to assess the structural origin of the problems. The sample geometries, specimen preparation, and results (where applicable) are given below for each of the four types of samples that were prepared.

## Experimental Procedures

Single crystal (110)-oriented  $\text{NdGaO}_3$  substrates were used for all of the samples described here. This material provides an excellent base for reliably depositing  $c$ -axis perpendicular YBCO films upon which, in turn, other films can be epitaxially grown. The sputter environment was made up of about half oxygen and half argon and the pressure was 20 millitorr. The presence of oxygen helps reduce contamination, although the oxygen can cause a problem with deposition depending on the relative positions of the sputter gun and the sample. With oxygen in the environment,  $\text{O}^-$  ions develop and are accelerated back towards the gun, interfering in the deposition process done by the positive ions. To avoid this problem, YBCO,  $\text{SrTiO}_3$ , and  $\text{PrBa}_2\text{Cu}_3\text{O}_{7-x}$  (PrBCO) layers were all off-axis deposited with the sputter gun perpendicular to the sample.

### *Step-edge S-N-S junctions*

For the step-edge structures, there are four layers deposited on the  $\text{NdGaO}_3$  substrate. In order of deposition (in other words, from the layer closest to the substrate to that which is farthest away at the top of the film), they are:

- 1) a  $c$ -perpendicular YBCO layer (100 nm),
- 2) a dual epitaxial insulating film used to isolate the two YBCO layers from each other, consisting of  $\text{SrTiO}_3$  (150 nm) and PrBCO (150 nm)
- 3) another  $c$ -perpendicular YBCO layer (100 nm)
- 4) a layer of gold (330 nm), which serves as the normal interlayer between the two superconducting YBCO films.

Deposition of each successive YBCO,  $\text{SrTiO}_3$ , PrBCO and YBCO layer was done using a GC Magnetron followed by lithography and patterning using 150 eV argon ion etching techniques in order to achieve the final geometry (Figure 1).

After deposition of the second and final YBCO layer, the sample was cooled to 100°C in 20 millitorr of dry oxygen, and then the oxygen was pumped out. Before the final layer of gold was deposited, a solution of 6% HF in  $\text{H}_2\text{O}$  was used to selectively wet-etch an undercut into the  $\text{SrTiO}_3$  layer (a 6% HF in  $\text{H}_2\text{O}$  solution will not etch the  $\text{NdGaO}_3$ , YBCO, or PrBCO layers). The use of the PrBCO layer was to allow the undercut into the insulating layer while at the same time avoiding etch-induced problems at the insulator/YBCO interface. After wet-etching, the gold was deposited using a 45° off-incident sputter gun angle. The entire processing sequence was carried out without breaking the vacuum and introducing air into the chamber. This eliminates contamination of the YBCO surface and helps to ensure a clean bond between the YBCO and the

gold. There is some unavoidable contamination of the metal by oxygen, but that was minimized as much as possible.

#### *Edge S-N-S junctions:*

These devices were fabricated in much the same way as the prior set of step-edge junctions. Once again, the layers were deposited by 90° off-axis sputtering, and the deposition and patterning processes were conducted consecutively without breaking vacuum. The tunnel barrier in this case is a layer of Co-doped YBCO. The geometry of the device is somewhat different for the edge junctions versus the previously-discussed step-edge configuration, as illustrated in Figure 2. In this case, no undercut was required.

#### *Specimen preparation for TEM:*

The TEM specimens were made from the chips as briefly described below. First, the chip was cut and bonded as illustrated in Figure 3 in order to make a 'sandwich'. An approximately 300  $\mu\text{m}$ -thick sample slice was then cut from the sandwich and thinned down to approximately 10-15  $\mu\text{m}$  using a Klepeis tripod polisher. Then the sample was ion milled in a Gatan ion mill at liquid nitrogen temperatures, using the sector speed control, at a low ion gun angle of 12° (see Figure 4) until perforation occurred. This method did require more time than some simpler approaches that were attempted, but it proved to be particularly successful when working with samples such as these which contain several diverse materials.

## **Results and Discussion**

#### *Step-Edge 1 (sample ID: T93-53-N6):*

Diffraction analysis of the individual layers in this chip confirms that the expected and desired relative epitaxial orientations were obtained, as shown in Figure 5. These selected area diffraction patterns were obtained by translation across a thin region between two edges that extended across the layered "island" structure from the upper YBCO layer (Fig. 5a) through the intervening PrBCO (Fig. 5b) and SrTiO<sub>3</sub> (Fig. 5c) layers and finally into the NdGaO<sub>3</sub> substrate (Fig. 5d).

The undercut proved to be successful in preventing short-circuiting of the device. As can be seen in Figure 6, the upper YBCO layer was not continuous in this sample. (For a corresponding schematic of the step-edge geometry, refer to Fig. 1.) Notice, however, that although the gold did deposit down into the undercut region, it failed to fill in the etched area completely. As a result, the gold layer was often discontinuous across the junction. This contributed to the poor electrical behavior of the chips.

Another problem that is illustrated in Fig. 6 is the inconsistent formation of the YBCO/PrBCO edges. The four separate devices shown in these micrographs should all exhibit the same shape of the insulator/superconductor stack, but instead we see that in some cases a smooth, continuous edge is present whereas in others the YBCO layer is smaller in the lateral dimension(s) and that this can produce a notch at the edge of the island. Figure 7a illustrates another formation problem found in this chip: an edge grain in the PrBCO which is out of epitaxial orientation. Figure 7b is a selected area diffraction pattern taken from the misoriented edge grain and Figure 7c is a selected area diffraction pattern taken from a region including both the epitaxial PrBCO, which makes up the bulk of the layer, and the rogue grain at the edge. Note that, at least in this case, the subsequent YBCO layer nonetheless appears to be a continuous film without any interior grain boundaries.

One final problem with the device synthesis identified in this investigation was the existence of some  $a$ -perpendicular regions in the YBCO layers away from the step-edges. These would be expected to reduce the total current that can be readily conducted through the layer due to the considerable in-plane vs. out-of-plane anisotropy of the YBCO superconductor. Most of these defects were present in pairs surrounding small particles on the surface (as illustrated in figure 8). Although the particles appear to be associated with the  $a$ - $\perp$  regions, it seems unlikely that they are directly responsible for nucleation of the  $c$ - $\perp$  to  $a$ - $\perp$  transition since the  $90^\circ$  boundaries extend much farther down in the film. No further analysis could be conducted at the time, and so the exact nature of the surface particles (misoriented YBCO? contaminant particles? subsequently deposited grains of gold?) is not yet known.

#### *Step-Edge 2 (sample ID: T93-81-UTEST9):*

Rather than belaboring the investigation of the defective structures described above, it seemed prudent to move on. An attempt was made to correct some of the problems by changes in processing parameters, as described below. Also, as per several recommendations from the P.I. and colleagues at Westinghouse, the student attempted to revise the TEM sample making process in the interest of reducing preparation time. These changes unfortunately resulted in TEM samples of inferior quality. Even though these samples were too thick to provide useful electron micrographs, *in situ* observations were made to determine whether or not the processing parameter changes made during chip fabrication were helpful.

Three main processing parameters were altered in order to try to correct the problems found in the first chip: gold sputter gun angle, deposition rate, and sputter pressure. An empirical investigation encompassing several combinations of variations in these parameters was carried out. The combination resulting in a sample with the best characteristics was selected, with the following relevant processing changes:

- 1) the sputter angle for the gold deposition was changed from 45° off of normal incidence to normal incidence,
- 2) the deposition rate was lowered to 100 Å/minute by reducing the power to the gun
- 3) the ambient pressure during sputtering was reduced from 20 millitorr to 5 millitorr

Upon examination of the samples, the most important effect of these changes was that the gold layer was continuous across the edges in this chip. The changing of the gun position angle is believed to have been the major factor in solving this problem. Furthermore, no  $\alpha$ -perpendicular regions were noticed in a preliminary survey.

The unexpected but major problem with this chip was that there was (surprise!) no undercut into the SrTiO<sub>3</sub>. As could be expected with no undercut, the original problem with the continuous YBCO layer did occur to some extent in this sample. The records showed that this chip had been wet-etched. It was determined at Westinghouse that the wet-etch process is dependent on the quality of the SrTiO<sub>3</sub>. SrTiO<sub>3</sub> with an X-ray rocking curve width of 0.7° or higher etches best, while SrTiO<sub>3</sub> with a narrow X-ray rocking curve width of 0.3° - 0.4° did not etch well. This substrate apparently fell into the latter category, and thus the undercut was not produced.

#### *Step-Edge 3 (sample ID: T93-94-UTEST15):*

The decision was made to make another chip with the same processing parameters as the previous one but to ensure that the step edges were undercut by wet-etching the sample for a long time. The success of the undercut was verified using scanning electron microscopy prior to making TEM samples. This way, the continuity of the gold across the edges could be confirmed for an undercut sample using a sputter gun angle normal to the incident.

Dr. Talvacchio (WSTC) was having problems with a persistent leak in their equipment and it took over a month for him to complete this chip and get it to Penn State. The only difference from the T93-81-UTEST9 chip is that the undercut was successful (as verified by SEM). The chip was processed and ready for TEM examination just before Thanksgiving 1993.

Due to additional high-priority work from other research groups within Westinghouse and other unforeseen circumstances, neither Ms. McGaughey nor Dr. Talvacchio could secure time for the pursuit of this project on the TEM at Westinghouse during December or January. As a result, this sample has not yet been examined.

#### *Edge 1 (sample ID: T93-99-A7):*

In order to make the best use of the available time, Dr. Talvacchio also sent another chip along for TEM preparation before T93-94-UTEST15 could be analyzed. This sample contained devices with the edge junction geometry described earlier and shown in Figure 2. A TEM sample

was prepared and was ready for examination just after Christmas. Once again, time on the TEM at Westinghouse was unavailable and so this sample has also not been analyzed.

## **Assessment**

One of the primary goals of this work was to use a knowledge of microstructural consequences to improve the processing of oxide superconductor devices. Valuable and unexpected insights concerning the device microstructures were in fact obtained by transmission electron microscopy. The initial problems with the devices were on a larger scale, such that the high-resolution aspects of the proposed work were not necessary or even appropriate for the examination of those issues. Unfortunately, once it appeared that initial fabrication problems had been ironed out and suitable devices had been made in which interfacial and defect structures would dominate the behavior, Ms. McGaughey could not obtain time on the high-resolution instrument at WSTC. Although the direct contact at Westinghouse (J. Talvacchio) also made repeated efforts to secure a slot for this work, the individuals responsible for the analysis equipment at WSTC were unable to provide any instrument time.

It should be noted that the student was understandably reluctant to examine the last several completed samples at lower resolution in the TEM at PSU, since the sample preparation is difficult and tedious. Good samples can easily become damaged by excessive handling. Even more likely is a build-up of contamination that destroys the utility of a sample if it is subjected to high-energy electrons in a mediocre to poor vacuum environment. Since this description applies to the Philips 420 at PSU, examination of the samples in that instrument would probably have made them unusable for subsequent high-resolution imaging.

Both the P.I. at Penn State (A. H. Carim) and the cognizant staff member at WSTC (J. Talvacchio) are nonetheless eager to obtain results from the remaining samples and bring this phase of the work to a more satisfactory conclusion. With the project support having terminated at the end of January, Dr. Talvacchio has tried to secure consulting funds and instrument time to allow Ms. McGaughey to examine the remaining specimens. At this point it appears that funds for 3-4 days of work will be available and that an arrangement may be possible for microscope time, despite the earlier problems.



## **Figure Captions:**

**Figure 1: YBCO step-edge junction chip (cross-sectional view).**

**Figure 2: YBCO edge junction chip with Co-doped YBCO barriers (cross-sectional views).**

**Figure 3: Cross-sectional sample "sandwich".**

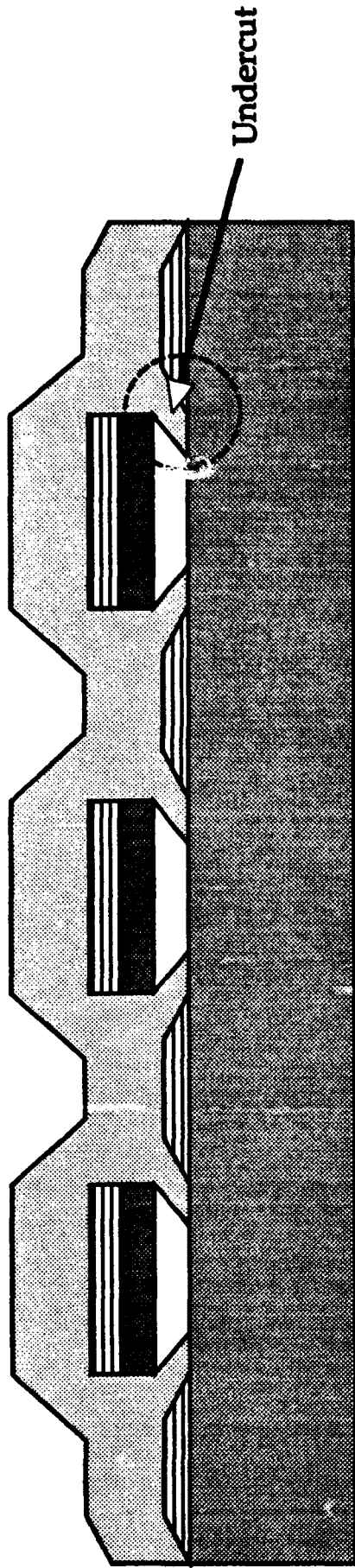
**Figure 4: Schematic of ion mill sample holder and its orientation.**

**Figure 5: Selected area diffraction patterns from adjoining areas in the (a) YBCO, (b) PrBCO, (c) SrTiO<sub>3</sub>, and (d) NdGaO<sub>3</sub>. The excellent epitaxy of the layers is evident.**

**Figure 6: Bright field micrographs of single step-edge junctions. Note that while the undercut succeeded in ensuring the discontinuity of the upper and lower YBCO regions, it also resulted in an undesirable loss of gold continuity across the junction.**

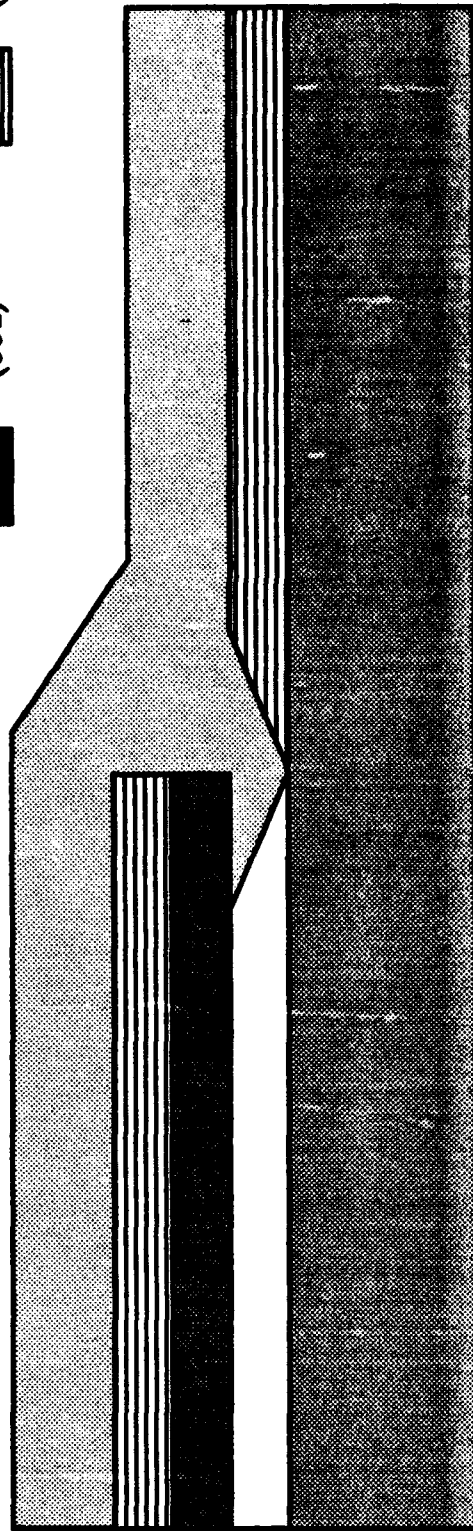
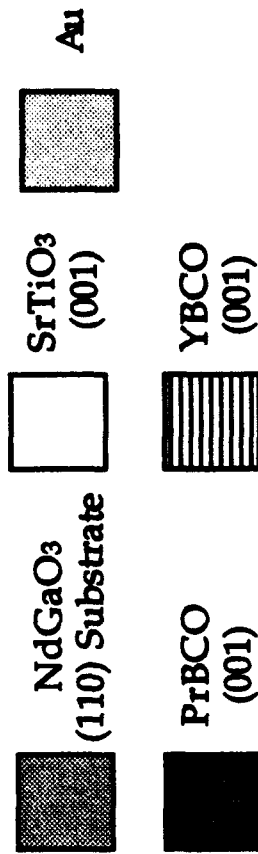
**Figure 7: (a) Bright field micrograph of a single step-edge junction with a misoriented edge grain in the PrBCO; (b) selected area diffraction pattern from the misoriented PrBCO grain; and (c) selected area diffraction pattern taken from an area including both the misoriented PrBCO edge grain and the epitaxial PrBCO.**

**Figure 8: Defective regions with the *a*-axis perpendicular within the YBCO.**



YBCO Step-Edge Junction (Multiple Steps)

Not To Scale



YBCO Single Step-Edge Junction (Cross-Sectional View)

Figure 1: YBCO Step-Edge Junction Chip  
(Cross-Sectional Views)

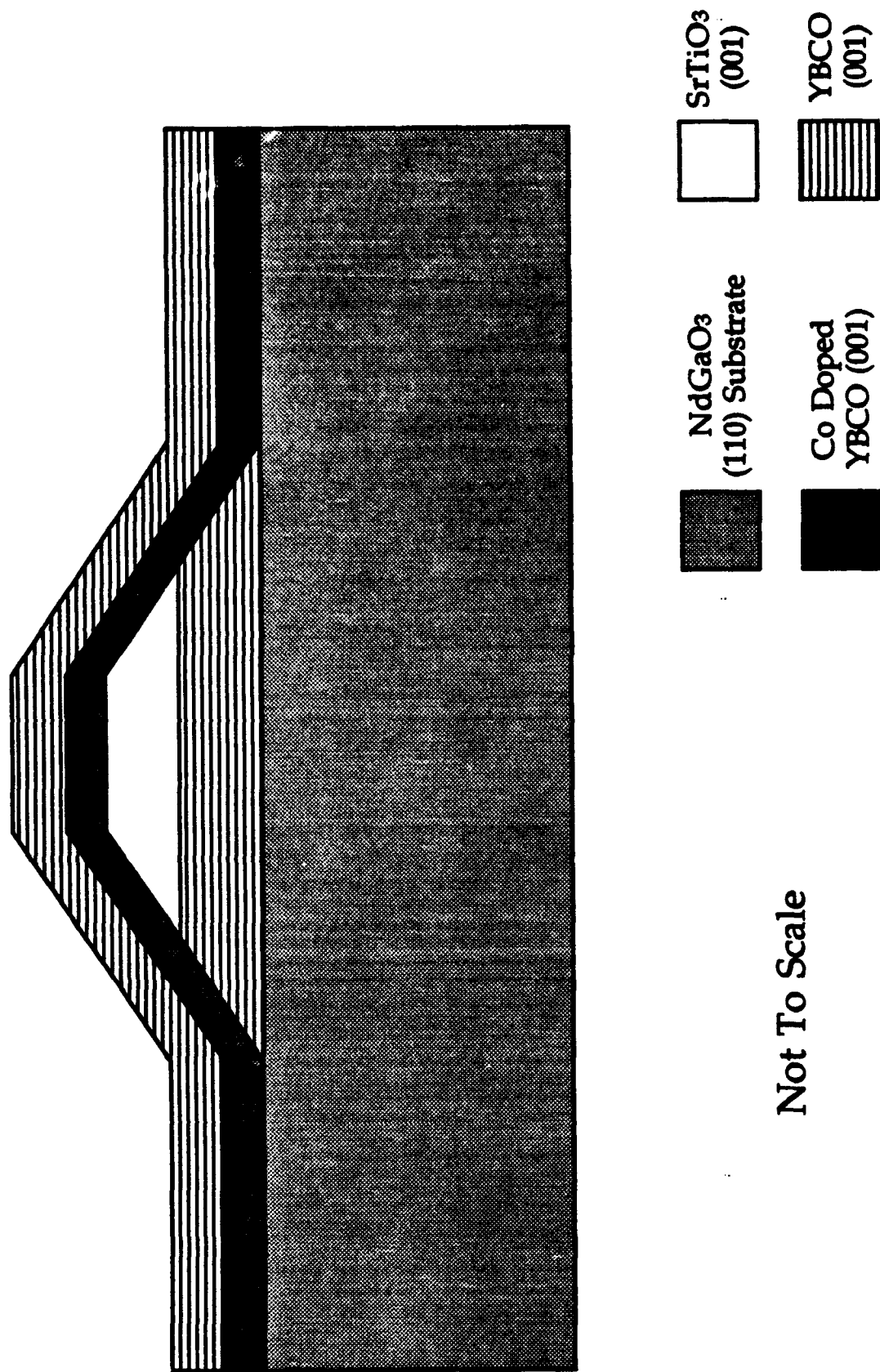


Figure 2: YBCO Edge Junction Chip with Co-Doped YBCO Barriers  
 (Cross-Sectional View)

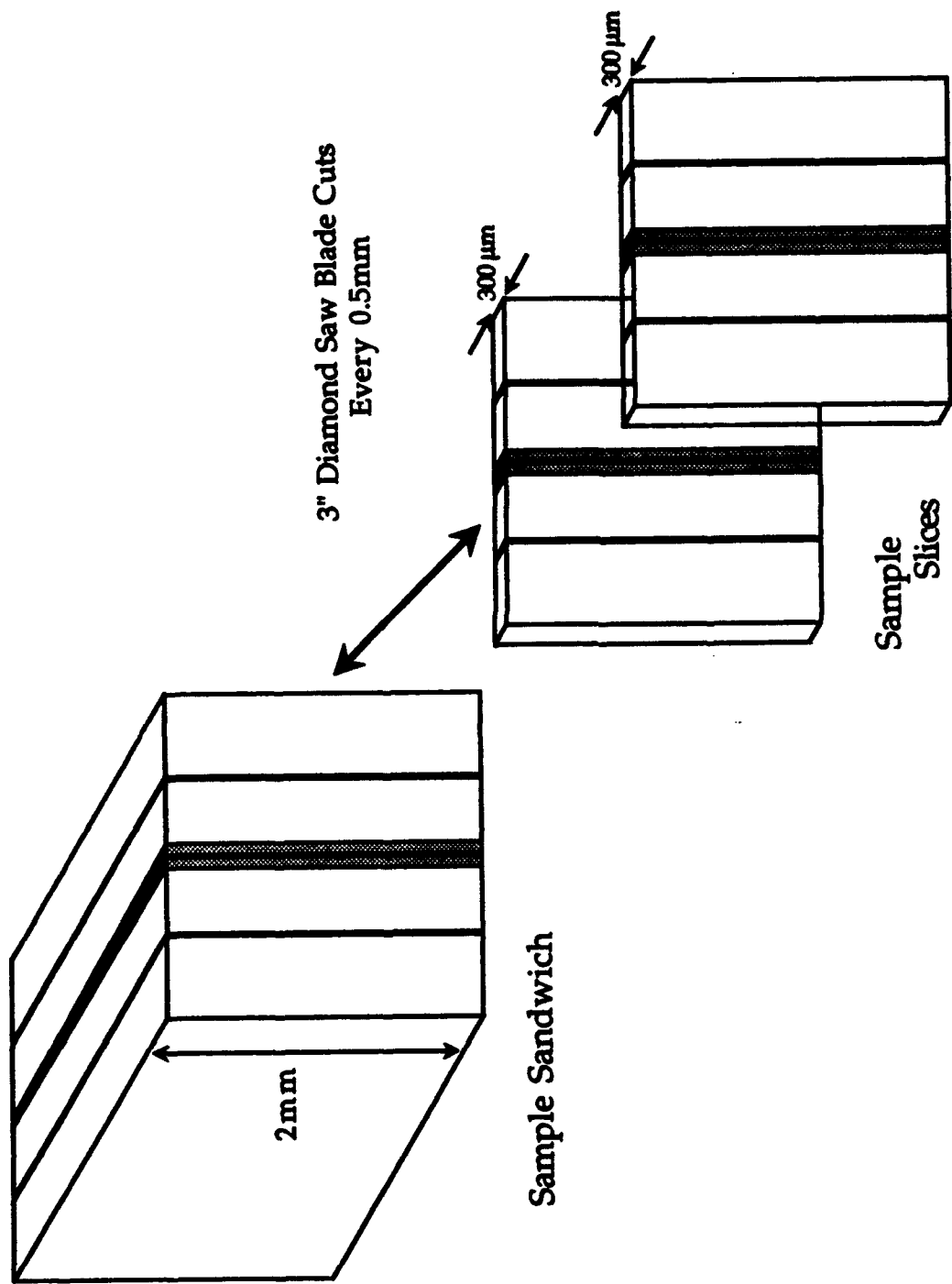


Figure 3: Cross-Sectional Sample 'Sandwich'

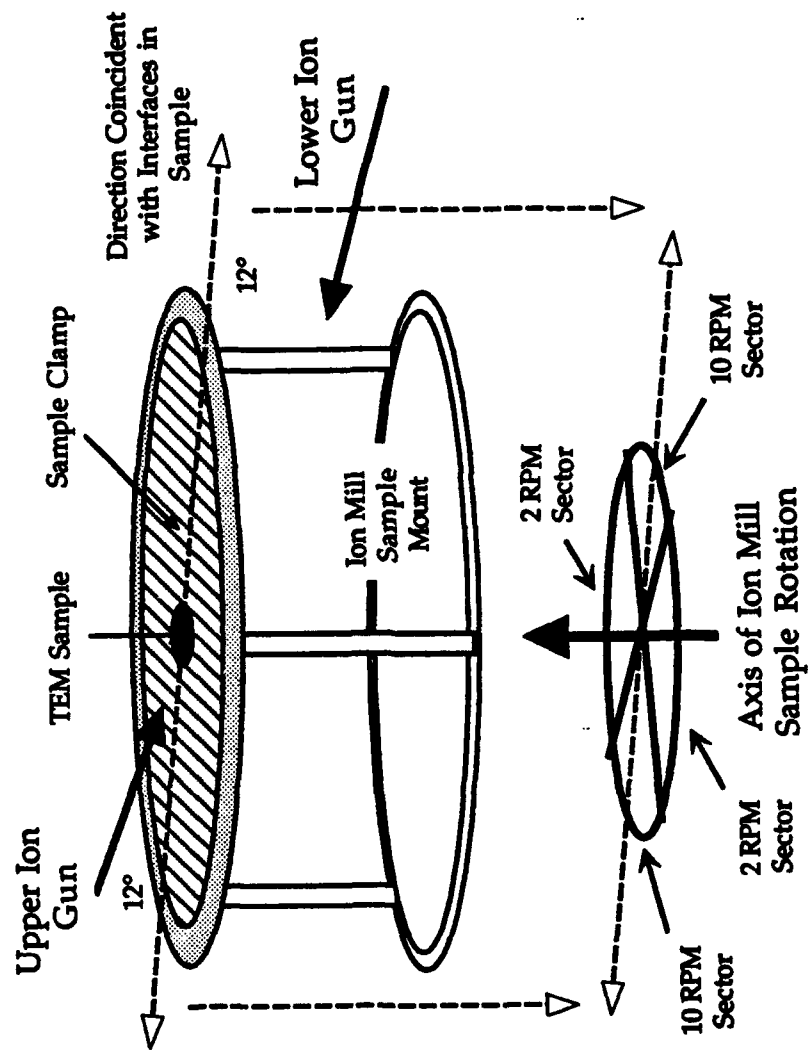


Figure 4: Schematic of Ion Mill Sample Holder and Milling Orientation

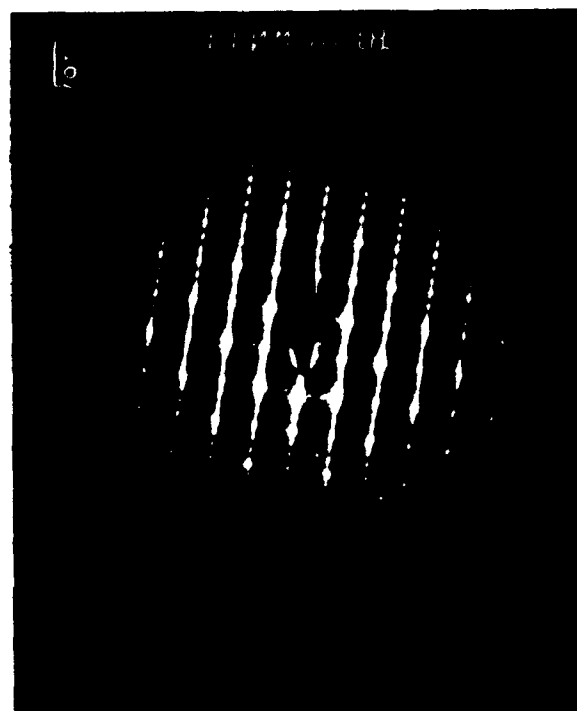
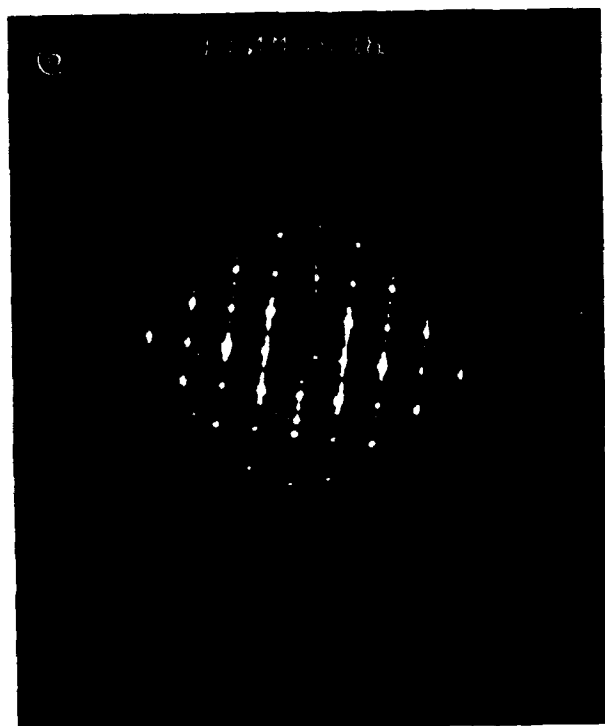


Figure 5

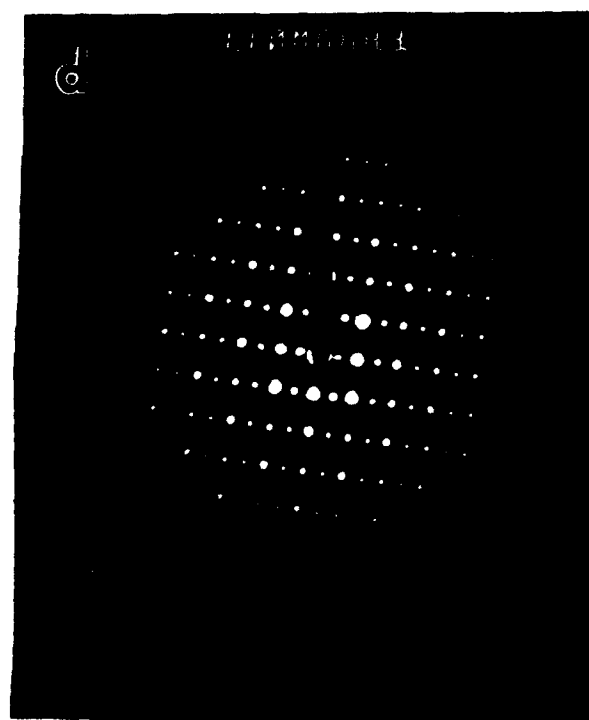
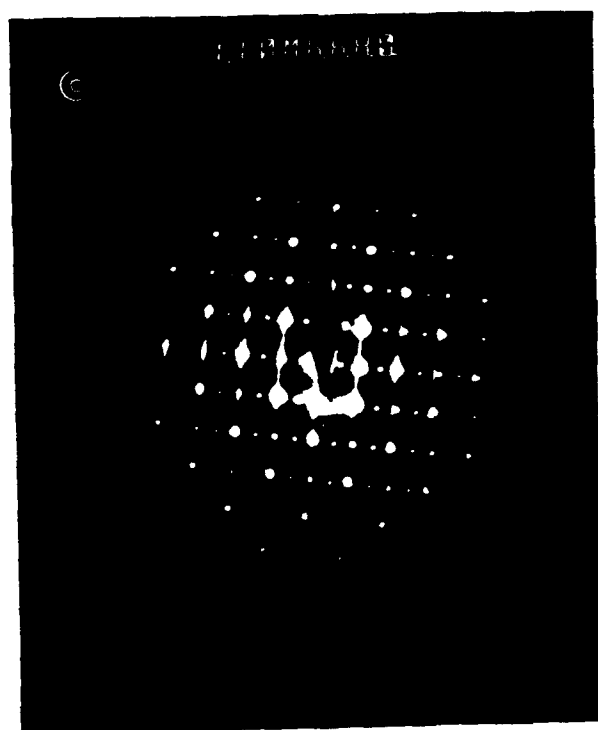




Figure 6



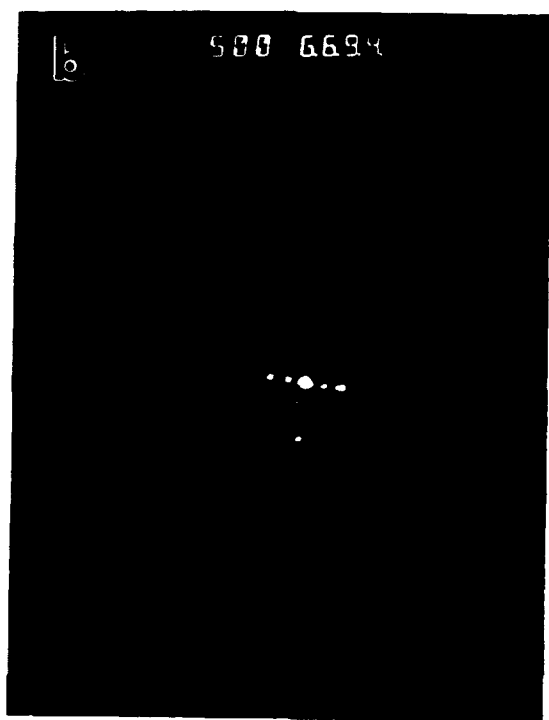


Figure 7





Figure 8